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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,824	10/26/2000	Omprakash S. Sarmaru	VELCP003	7360

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ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,824	SARMARU ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/26/00;12/28/00;6/26/01;8/31/01;4/3/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-16, 18-21* is/are rejected.

7)☒ Claim(s) *7 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the abstract is written in two paragraphs. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

In the cross reference to related application section, the applicant is advised to update the "co-pending Provisional Application" as "expired Provisional Application" and remove the Attorney Docket number.

The summary of invention section is in the specification is missing.

All the acronyms must be written in full at least once in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3, 5, 18, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 3, the limitation "logic for correlating the upstream packets and downstream packets" is failed to point out the exact degree of correlating between upstream and downstream packets. For examination purposes, the examiner considers the above limitation as a logic for converting the upstream packets to the downstream packets by network protocol between nodes.

Re claim 5, the limitation "the selected subsets" lacks an antecedence basis. For examination purposes, the examiner considers this limitation as "the Y rows". Thus, claim 18 also has the same problem.

Re claim 21, the limitation "the correlating act" lacks an antecedence basis. For examination purposes, the examiner disregards this limitation because the claim language does not clearly state the meaning of above limitation.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6, 8-16, and 18-21 are rejected under 35 U.S.C. 103(a) as being obvious over Mannering et al. (U.S. 6,137,839) in view of Gossett et al. (U.S. 6,230,177).

Re claim 1, Mannering et al. disclose a Fourier transform processor (abstract) comprising: a) an input sample delivery circuit for delivering a sample set of a one of N (100 in Figure 3a as a modem for receiving and transmitting samples), time domain samples and Nr frequency domain samples (Figure 6f) in a row and column order, and a xDSL circuits in Figure 2a comprising an input sample delivery circuit for delivering the samples (modem interface cards) and at least one sliced radix circuit (multiple DSP and Protocol processor cards). Mannering et al. do not disclose the 2-dimension FFT wherein at least one row and column circuit with an input and an output, and the row and column circuit performing a row and column transform on complex valued samples at the input to produce at the output coefficients corresponding with an other of the time domain and the frequency domain; and at least one sliced radix circuit of order "R" with R parallel inputs and an output coupled to the input of at least one row and column circuit, and at least one sliced radix circuit transforming Nj /R input samples from the sample set into a selected one among the R possible complex outputs. However, Gossett et al. discloses in Figures 1, 4, and 12 a 2-dimension FFT wherein at least one row and column circuit (Figure 4) with an input (left input data to 401) and an output (right output data (404), and the row and column circuit performing (col. 2 lines 60-65) a row and column transform on complex valued samples at the input to produce at the output coefficients corresponding with an other of the time domain (f(n)) and the frequency domain (F(k)); and at least one sliced radix circuit (Figure 12) of order "R" with R parallel inputs (R = 4) and an output

coupled to the input of at least one row and column circuit (output of Figure 12), and at least one sliced radix circuit transforming Nj /R input samples (f(n), f(M+n), f(2M+n), and f(3M+n)) from the sample set (f(n)) into a selected one among the R possible complex outputs (Complex multiply and col. 5 lines 39-46). Therefore, it would have been obvious for a person having ordinary skill in the art at the time the invention is made to add a 2-dimension FFT with detail structure, specially the sliced radix circuit, as described by Gossett et al.'s invention into Mannering et al.'s invention because it is a key operation in many application domain including DSP for improving the system performance in real-time (col. 1 lines 57-64 in Gossett et al.'s invention).

Re claim 2, Mannering et al. further disclose in Figure 13 a input sample delivery circuit further comprises: a downstream communication circuit (bottom portion of Figure 6e) for processing downstream packets each including a respective frequency domain sample set of a portion of a channel of data to destined for a subscriber (Figure 13a and col. 39 lines 10-17); an upstream communication circuit (upper portion of Figure 6e) for processing upstream packets each including a respective time domain sample set of a portion of a channel of data from a subscriber (an architecture of DSL in Figure 2b); and an input memory for consecutive delivery of each of sample sets (36 in Figure 4a).

Re claim 3, Mannering et al. further disclose input sample delivery circuit further comprises: logic for correlating the upstream packets and downstream packets with a corresponding protocol together with a variable size N (Figure 11c wherein the protocol is either Telnet, FTP, HTTP...), of each of the sample sets on the basis of a corresponding indicia within each of the upstream and downstream packets (Figure 14b

and Figure 10f); and logic for configuring each of at least one row and column circuit together with at least one sliced radix circuit responsive to the correlating of logic for correlating (Figure 4a).

Re claim 4, Mannering et al. further discloses the down stream packets and upstream packets collectively include more than one X-DSL communication protocol (Figure 11c wherein x-DSL communication protocol including Telnet, FTP, Netscape "HTTP").

Re claim 5, Mannering et al. do not disclose input sample delivery circuit further comprises: logic for folding the set of Nr samples into a first two dimensional array of Y rows and X columns, logic for decomposing each of the Y rows into a second two dimensional to array with R columns corresponding in a number with the order of the radix and Z rows, and with each of the Z rows comprising one of the selected subsets and with each sample within each of the Z rows corresponding with an interleaving of a corresponding one of the Y rows at a sample separation substantially equal to X/R. However, Gossett et al. disclose in Figures 4 and 6 logic for folding the set of Nr samples (front face of data in Figure 6) into a first two dimensional array of Y rows (vertical data) and X columns (horizontal data), logic for decomposing each of the Y rows into a second two dimensional to array with R columns (401) corresponding in a number with the order of the radix and Z rows (403), and with each of the Z rows comprising one of the selected subsets and with each sample within each of the Z rows corresponding with an interleaving of a corresponding one of the Y rows at a sample separation substantially equal to X/R (col. 20 lines 6-10). Therefore, it would have been obvious to a person

having ordinary skill in the art at the time the invention is made to add the 2-dimension FFT with a logic for folding the set of N samples and a logic for decomposing each of the rows data into 2-dimensional FFT as described in Gossett et al.'s invention into Mannering et al.'s invention because it is a key operation in many application domain including DSP for improving the system performance in real-time (col. 1 lines 57-64 in Gossett et al.'s invention).

Re claim 6, Mannering et al. do not disclose the input sample delivery circuit further comprises: logic for determining that a sample set of Ni samples includes exclusively real valued time domain samples; and logic for compressing the sample set to N, samples by expressing corresponding pairs of real values samples as a single complex valued sample, wherein N, substantially equals half of Ni. However, Gossett et al. disclose in Figure 3 logic for determining that a sample set of Ni samples (Wa, Wp, W2p, and W3p) includes exclusively real valued time domain samples; and logic for compressing the sample set to N, samples by expressing corresponding pairs of real values samples as a single complex valued sample ({first two output} and {last two output}), wherein N, substantially equals half of Ni (Ni = 4 and N = 2). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a real to complex compressor as described above by Gossett et al.'s invention into Mannering et al.'s invention because it is a typical process of an FFT in the art and it would enable to simplify the hardware complexity to modulate the carrier with low power consumption.

Re claim 9, Mannering et al. do not disclose at least one row and column circuit further performs a row transform of an order X and a column transform of an order X + R. However, Gossett et al. disclose in Figure 4 at least one row and column circuit further performs a row transform of an order X (L = X) and a column transform of an order X + R (M = X+ R = L + R). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add at least one row and column circuit further performs a row transform of an order X and a column transform of an order X + R as disclosed by Gossett et al.'s invention into Mannering et al.'s invention because it would enable to perform FFT in the system faster.

Re claim 10, Mannering et al. disclose multiple DSP cards in the modem in Figure 1e (100). Mannering et al. fail to disclose a first and second sliced radix circuit of the order R with R parallel inputs coupled to input sample delivery circuit and an output, and first sliced radix circuit transforming N, /R to input samples from the sample set into a first selected one among the R possible complex outputs. However, Gossett et al. disclose in Figure 12 a sliced radix circuit of the order R with R parallel inputs (R = 4) coupled to input sample delivery circuit (f(x)) and an output (output), and first sliced radix circuit transforming N/R to input samples from the sample set into a first selected one among the R possible complex outputs (Complex Multiply). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to include first and second sliced radix circuit as disclosed by Gossett et al.'s invention into Mannering et al.'s invention because it would enable to improve the system performance by processing multiple data simultaneously.

Re claim 11, Mannering et al. further disclose at least one sliced radix circuit includes: a summer with R parallel inputs and an output (col. 42 lines 25-26), and the summer summing all of the parallel inputs to generate the output; scalars (col. 42 lines 43-45 and 40-42) for scaling requisite ones of the R parallel inputs to by a selected one of the R subsets of scale factors associated with a radix R transform; a multiplier for multiplying sums output by summer by a corresponding twiddle factor to produce the selected one among the R complex outputs (FFT processor and col. 42 lines 25-26).

Re claim 12, it is a method claim of claim 1. Thus, claim 12 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 13, it is a method claim of claim 2. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 14, it is a method claim of claim 4. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 15, it is a method claim of claim 5. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 16, it is a method claim of claim 6. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 17, it is a method claim of claim 7. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 18, it is a method claim of claim 5. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 19, it is a method claim of claim 10. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 20, it is a method claim of claim 5. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 21, it is a method claim of claim 9. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 9.

Allowable Subject Matter

8. Claims 7 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,240,141 to Long discloses a lower-complexity peak-to-average reduction using intermediate-result subset sign-inversion for DSL.

b. U.S. Patent No. 6,401,162 to Nasserbakht discloses a generalized fourier transform processing system.

c. U.S. Patent No. 6,334,219 to Terrance discloses a channel selection for a hybrid fiber coax network.

d. U.S. Patent No. 6,055,268 to Timm et al. disclose a multimode digital modem.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

June 3, 2003

CHUONG DINH NGO
PRIMARY EXAMINER